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System-Level Power Loss Evaluation of Modular Multilevel Converters

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***Abstract*—For modular multilevel converters (MMCs), reducing the design margin while fulfilling the reliability target in the design stage is challenging. To address this challenge, a system-level power loss evaluation is essential. Although many studies have discussed the power loss calculation of the MMC, most of them focus on the power losses of semiconductor devices while ignoring the impact of capacitors, arm inductors, and ac transformers. Therefore, this paper proposes a system-level power loss evaluation for MMCs from the perspective of reliability assessment. The power loss model covers switching devices, capacitors, and inductors. All the power loss calculation is starting from the active/reactive-power set points of the converter at the point of common coupling (PCC), where the converter is connected to the AC grid. The leakage inductance of the ac transformer is also considered. In addition, in order to meet the needs of long-term reliability assessment, the proposed power loss calculation is computation-efficient and easy to update parameters. The theoretical analysis has been verified by a full-scale MMC in simulations and a down-scale platform by experiments.**

I. Introduction

The modular multilevel converter (MMC) has distinctive features of modularity, scalability, superior harmonic performance, low switching stresses [1], etc. However, the MMC is a large-scale and complex system. Hundreds or thousands of individual components, including insulated-gate bipolar transistors (IGBTs), capacitors, inductors must operate properly. For example, the first commercial MMC-HVDC project–Trans Bay Cable project has 216 submodules (SMs) per arm [2]. Over 1,000 capacitor banks and more than 2,000 IGBT modules are employed in the system. Any unexpected failures might lead to shut-down of the whole system and lower its availability. From this perspective, reliability is of great importance to the design and operation of the MMC.

To improve the reliable performance of the MMC, sizing components with excessive design margins is a widely accepted solution in the industry. In addition, various redundancies are applied [3]. Nonetheless, the design constraints in cost and efficiency impose a great challenge on the application of MMCs. How to design an MMC with compromised costs and design margins while fulfilling a specific reliability target is still an open question. To do it confidently, a reliability analysis-oriented power loss evaluation for the whole MMC system is a prerequisite.

One of the widely used methods for loss evaluation of the MMC is numerical solutions based on simulations. In the analysis of an established MMC station, the international standard IEC-62751-2 recommends using simulation methods to achieve a 3% uncertainty [4]. Moreover, some simplified simulation methods are proposed in [5] to improve computational efficiency. Numerical solutions have advantages of considering sophisticated degrees of freedom in terms of control strategies in the MMC. However, different cases rely on the modification of the simulation parameters. When comparing the reliable performance of different design schemes (e.g., selection of device parameters, device types, and the number of submodules (SM)), the simulation-based methods are challenging to change these parameters fast and automatically.

An alternative approach is to establish analytical models to estimate the power losses of the MMC [6]–[12]. Reference [6] provides analysis of semiconductor power losses on the basis of a new modulation scheme. Afterward, based on the conduction path of the arm current, reference [7] proposes to utilize an inserted probabilities of each SM to calculate the power semiconductor losses of the MMC. Different SM topologies have also been evaluated in the inserted probability method [8]. Regarding the variable switching frequency of the MMC under nearest-level modulation (NLM), reference [9] presents an analytical method to estimate the switching power losses of the MMC. Furthermore, the impacts of other parameters, such as junction temperatures [10], grid integration [11], the use of new devices [12], etc., are also considered. However, all the aforementioned methods focus on the power semiconductor devices only. The capacitors and inductors, which contribute to the system-level reliability of the MMC, have been rarely discussed. Moreover, it is worth mentioning that the reactive power consumption of the leakage inductance of the ac transformer should not be ignored in the power loss analysis. Although it is not necessary to have a higher value of phase inductance as a filter, the transmission transformer has 0.14 p.u. leakage inductance typically given the manufacturing cost [13].

This paper proposes a system-level power loss evaluation for the MMC, which considers the switching devices, capacitors, and inductors. The established model is computationally efficient, friendly to parameters changing as well as considering the leakage inductance of the transmission transformer. Moreover, a down-scale MMC platform has been built. The established analytical model is experimentally verified.

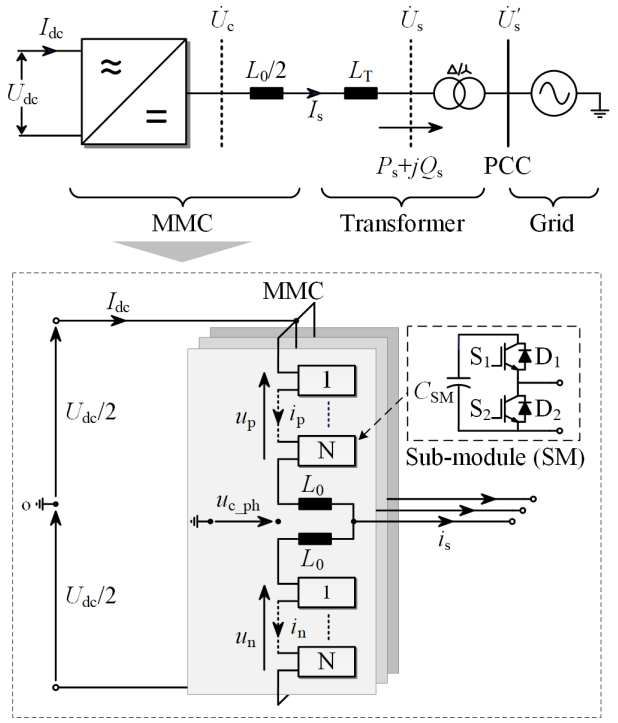


Fig. 1. The configuration of an MMC interfaced to an ac system through a transformer.

II. An MMC Configuration Connecting with Power Grids

The configuration of an MMC interfaced to an AC system through a transformer is shown in Fig. 1, where L_T is the leakage inductance of the transformer, and L_0 is the arm inductor. The leakage inductance of a transmission transformer is typically 0.14 p.u. Therefore, the voltage across the transformer cannot be ignored when calculating the internal voltage within the converter. In addition, any active/reactive power calculation should be referenced to the (PCC) with the AC grid, rather than the converter terminals.

In this work, the grid voltage at the virtual point of the secondary transformer is selected as the reference. Then, the grid voltage and the line-to-line AC voltage of the converter are expressed as

$$\dot{U}_s = \hat{U}_s \angle 0°,\ \dot{U}_c = \hat{U}_c \angle \delta \tag{1}$$

where $\hat{U}_s$ and $\hat{U}_c$ are the grid voltage amplitude and the converter ac voltage amplitude, and δ is the power angle, which is the phase angle between U_c and U_s.

The phase reactance is a combination of the transformer leakage reactance and the arm reactance, which is

$$L_{eq} = L_T + L_0/2 \tag{2}$$

where L_T is the transformer leakage reactance and L_0 is the arm reactance. Although it is not necessary to have a high value of phase reactance as a filter in the MMC, the phase reactance is still typically around 0.14 p.u. in the real project given the manufacturing cost [13].

Modulation index is defined as the ratio of the amplitude of the converter phase voltage by the half the dc bus voltage, which is given by

$$m = \frac{\hat{U}_{c\_ph}}{U_{dc}/2} = \frac{2\hat{U}_c}{\sqrt{3}U_{dc}} \tag{3}$$

where $\hat{U}_{c\_ph}$ is the amplitude of the converter phase voltage, U_{dc} is the dc bus voltage, and $\hat{U}_c$ is the amplitude of line-to-line voltage at the converter terminal.

Active and reactive powers of the PCC (X_{eq} is the impedance of the phase reactance) are obtained as

$$\begin{cases} P_s = \dfrac{U_s U_c \sin\delta}{X_{eq}} \\ Q_s = \dfrac{U_s\left(U_c\cos\delta - U_s\right)}{X_{eq}} \end{cases} \tag{4}$$

Substituting (4) into (3), the modulation index of the MMC is thus solved by

$$m = \frac{2\sqrt{2}}{\sqrt{3}}\frac{\lambda U_s}{U_{dc}} = \frac{2\sqrt{2}\left(Q_s X_{eq} + U_s^2\right)}{\sqrt{3}U_{dc}U_s\cos\delta} \tag{5}$$

which indicates that the modulation index is not changed freely when the MMC is connected to the grid. The grid parameters (e.g., reactive power, grid voltage, etc.) determine the range of modulation index. Therefore, the phase voltage at the converter terminal and the AC current are expressed according to Fig. 1 as

$$\begin{cases} u_{c\_ph}(t) = \dfrac{m}{2}U_{dc}\sin(\omega t) \\ i_s(t) = \sqrt{2}I_s\sin(\omega t - \varphi_c) \end{cases} \tag{6}$$

where φ_c is the phase angle given by the converter ac voltage, which $\varphi_c = \delta + \varphi$.

In the steady-state, the arm currents are expressed as

$$i_p(t) = \frac{I_{dc}}{3} + \frac{\hat{I}_s}{2}\sin(\omega t - \varphi_c) = \frac{\hat{I}_s}{2}\left[k + \sin(\omega t - \varphi_c)\right] \tag{7}$$

$$i_n(t) = \frac{I_{dc}}{3} - \frac{\hat{I}_s}{2}\sin(\omega t - \varphi_c) = \frac{\hat{I}_s}{2}\left[k - \sin(\omega t - \varphi_c)\right] \tag{8}$$

where k is the current ratio in arm currents, which is defined as

$$k = \frac{I_{dc}}{3}\Big/\frac{\hat{I}_s}{2} \tag{9}$$

Considering an ideal MMC model with N SMs per arm, the insertion probability of the upper arm and lower arm are denoted by N_p and N_n as

$$\begin{cases} N_p = \dfrac{u_p}{NU_{SM}} = \dfrac{1}{2}\left[1 - m\sin(\omega t)\right] \\ N_n = \dfrac{u_n}{NU_{SM}} = \dfrac{1}{2}\left[1 + m\sin(\omega t)\right] \end{cases} \tag{10}$$

As of now, all MMC control variables (e.g., modulation index, arm voltages/currents) have been established based on the analytical relationship according to the P/Q set points of PCC with the AC grid.

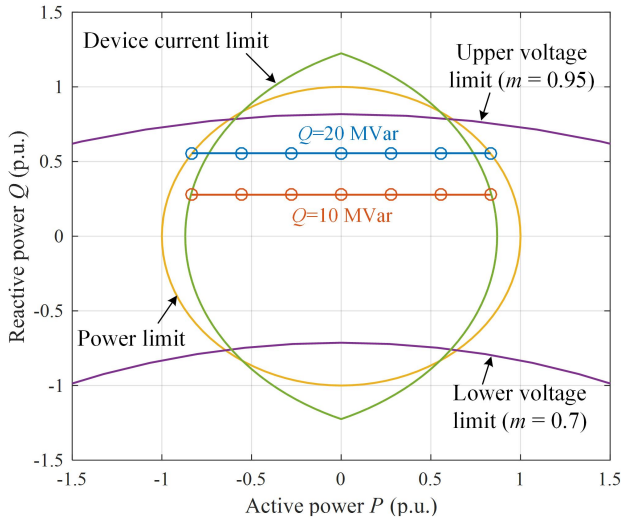


Fig. 2. Active and reactive power capability (P/Q circle) graph of a full-scale MMC with different component and system limitations.

TABLE I
PARAMETERS OF A 36-MVA MMC USED A CASE STUDY.

Parameters Symbols	Values and units
Nominal apparent power S_{N}	36 MVA
Nominal active power P_{N}	30 MW
DC bus voltage U_{dc}	30 kV
Switching frequency f_{sw}	333 Hz
Leakage reactance of the transformer L_{T}	2.8 mH (0.14 p.u.)
Arm reactance L_0	2.4 mH (0.12 p.u.)
Equivalent inductor resistance $R_{\mathrm{sL\_dc}}$, $R_{\mathrm{sL@50Hz}}$	20 mΩ, 21.9 mΩ
SM capacitance C	2.65 mF
Capacitor series resistance is R_{sC}	0.47 mΩ
Dielectric loss tangent is $\tan\delta_0$	3×10^{-4}
Grid line voltage at PCC U_{s}	15 kV
Nominal grid current I_{s}	1.38 kA
Number of SMs per arm N	10
Bleeding resistor of each SM R_{b}	4.5 kΩ

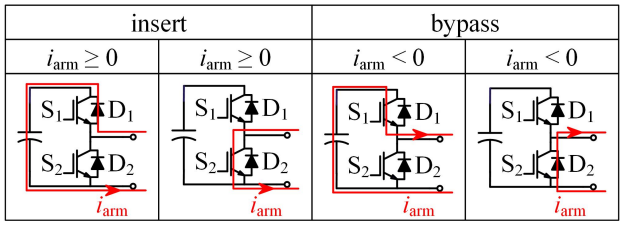


Fig. 3. The operating diagram of an SM in the MMC system.

III. POWER LOSSES OF CRITICAL COMPONENTS IN A FULL-SCALE MMC

In this section, a full-scale MMC is selected as a case study for power loss evaluation. The parameters of the MMC are listed in Table I. Varies active power points (-30 MW–30 MW) and reactive power points (10 MVar and 20 MVar) are selected in simulation. All of these operating points are located in the P/Q capability circle as shown in Fig. 2.

TABLE II
THE AVERAGE AND RMS CURRENTS OF THE FOUR POWER DEVICES IN AN SM OF THE MMC

	Average current (A)
S_1	$\frac{\hat{I}_{\mathrm{s}}}{4\pi}\left(k^2-1\right)\cos\alpha$
D_1	$\frac{\hat{I}_{\mathrm{s}}}{4\pi}\left(1-k^2\right)\cos\alpha$
S_2	$\frac{\hat{I}_{\mathrm{s}}}{4\pi}\left[\left(\pi+2\alpha\right)k+\left(1+k^2\right)\cos\alpha\right]$
D_2	$\frac{\hat{I}_{\mathrm{s}}}{4\pi}\left[\left(\pi-2\alpha\right)k-\left(1+k^2\right)\cos\alpha\right]$
	The power of RMS current (A^2)
S_1	$\frac{\hat{I}_{\mathrm{s}}^2}{16\pi}\left[\left(\frac{1}{2}-k^2\right)\left(\pi-2\alpha\right)-\frac{k}{3}\cos\left(3\alpha\right)\right]$
D_1	$\frac{\hat{I}_{\mathrm{s}}^2}{16\pi}\left[\left(\frac{1}{2}-k^2\right)\left(\pi+2\alpha\right)+\frac{k}{3}\cos\left(3\alpha\right)\right]$
S_2	$\frac{\hat{I}_{\mathrm{s}}^2}{16\pi}\left[\left(\frac{1}{2}+3k^2\right)\left(\pi+2\alpha\right)+6k\cos\alpha-\frac{k}{3}\cos\left(3\alpha\right)\right]$
D_2	$\frac{\hat{I}_{\mathrm{s}}^2}{16\pi}\left[\left(\frac{1}{2}+3k^2\right)\left(\pi-2\alpha\right)-6k\cos\alpha+\frac{k}{3}\cos\left(3\alpha\right)\right]$

A. Power Losses of the Power Semiconductor Modules

In the full-scale MMC system, a 4500 V/1200 A IGBT module is selected (ABB 5SNA-1200G450350), where the composition of power losses are dominated by the conduction and switching losses.

According to [14], the conduction losses of IGBT modules are calculated by

$$P_{\mathrm{cond}} = \left|I_{\mathrm{avg}}\right|\left[U_{\mathrm{cond0@}T_{\mathrm{ref}}} + K_{\mathrm{T1}}\left(T_j - T_{\mathrm{ref}}\right)\right] + I_{\mathrm{RMS}}^2\left[r_{\mathrm{cond0@}T_{\mathrm{ref}}} + K_{\mathrm{T2}}\left(T_j - T_{\mathrm{ref}}\right)\right] \quad (11)$$

with $U_{\mathrm{cond0@}T_{\mathrm{ref}}}$, $r_{\mathrm{cond0@}T_{\mathrm{ref}}}$, K_{T1} and K_{T2} being the coefficients obtained from the datasheet. T_{ref} is the reference temperature, typically at 25°C or 125°C. In addition, I_{avg} and I_{RMS} are the average current and the rms current flowing through the power devices.

Switching energy dissipations $E_{\mathrm{sw}} = E_{\mathrm{on}} + E_{\mathrm{off}}$ for the IGBT and $E_{\mathrm{sw}} = E_{\mathrm{rr}}$ for the freewheeling diode on the current I, junction temperature T_{j} and blocking voltage U_{cc} are given by

$$E_{\mathrm{sw}} = E_{\mathrm{swref}}\cdot\left(\frac{I}{I_{\mathrm{ref}}}\right)^{K_i}\cdot\left(\frac{U_{\mathrm{cc}}}{U_{\mathrm{ccref}}}\right)^{K_u}\cdot\left[1+TC_{\mathrm{sw}}\left(T_{\mathrm{j}}-T_{\mathrm{ref}}\right)\right] \quad (12)$$

with E_{on}, E_{off} and E_{rr} being the turn-on, turn-off and reverse recovery energy per pulse provided in the datasheet. I_{ref}, U_{ccref}, T_{jref} and E_{swref} are the nominal test conditions. K_i, K_u and TC_{sw} are coefficients obtained from the datasheet. Note that the device current I is the instantaneous current.

The average switching losses of the IGBT and the diode are

$$P_{\mathrm{sw\_S}} = \frac{1}{T}\sum_{t_0}^{t_0+T} E_{\mathrm{sw}}\left(i_{\mathrm{CE}}\right) \quad (13)$$

$$P_{\mathrm{rec\_D}} = \frac{1}{T}\sum_{t_0}^{t_0+T} E_{\mathrm{sw}}\left(i_{\mathrm{f}}\right) \quad (14)$$

where $P_{\mathrm{sw\_S}}$ and $P_{\mathrm{rec\_D}}$ are the average switching losses during a fundamental period T, i_{CE} and i_{rec} are the instantaneous device currents for IGBT and diode, respectively.

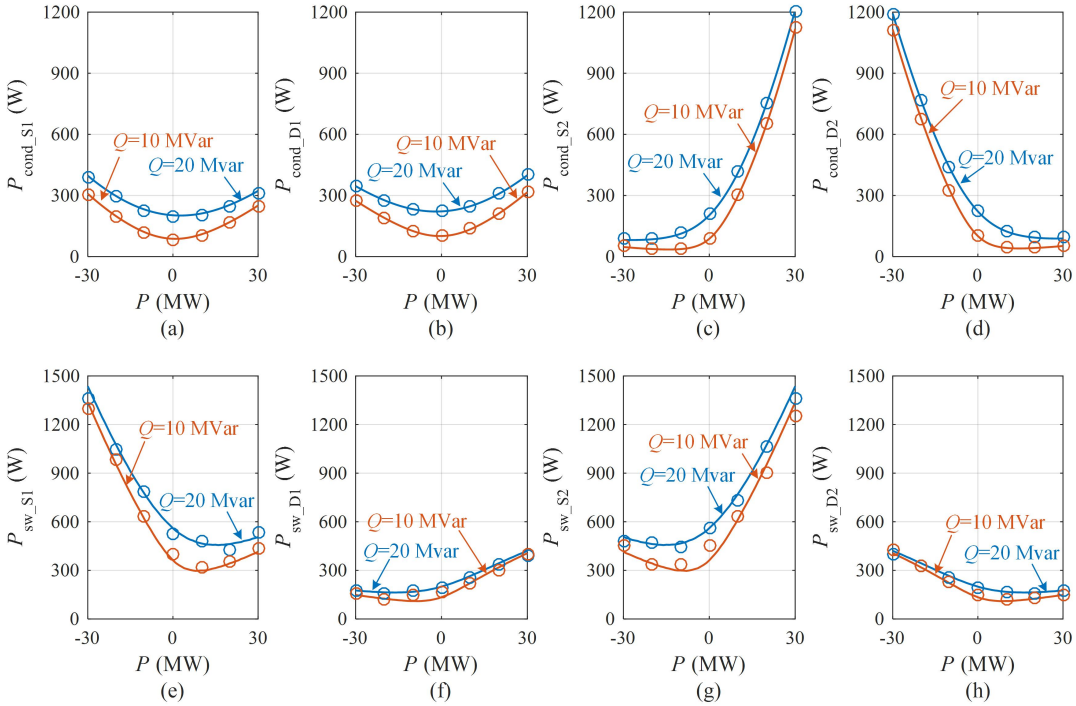


Fig. 4. Comparison of the conduction and switching power losses of four power devices in an SM under different P/Q set points, where the smooth curves are theoretical results and the dots "○" are simulated results: conduction and switching power losses of the device S_1 (a) and (e), D_1 (b) and (f), S_2 (c) and (g), and D_2 (d) and (h).

Based on (11)–(14), one of the key points to calculate the power losses of the IGBT module is to find the instantaneous current, average current and the RMS current flowing through the power devices. As shown in Fig. 3, when the arm current is positive, the current flows through the devices D_1 and S_2. On the contrary, the arm current passes through the devices S_1 and D_2 with a negative current. Therefore, it is necessary to calculate the zero points of the arm current. Solving (7), the zero points of the arm currents are expressed as

$$\begin{cases} \omega t_1 = -\alpha + \varphi_c \\ \omega t_2 = \pi + \alpha + \varphi_c \end{cases}, \text{ where } \alpha = \arcsin(k) \tag{15}$$

According to the conduction times of the switches and the characteristics under the non-conduction state, the instantaneous, the average and the square of RMS currents of the device S_1 are calculated as

$$i_{\text{CE\_S1}} = \begin{cases} 0, & 2\pi + \omega t_1 \leqslant \omega t < \omega t_2 \\ N_p i_p, & \omega t_2 \leqslant \omega t < 2\pi + \omega t_1 \end{cases} \tag{16}$$

$$I_{\text{S1\_avg}} = \frac{1}{2\pi}\int_{\omega t_2}^{2\pi+\omega t_1} N_p i_p d\omega t = \frac{\hat{I}_s}{4\pi}\left(k^2-1\right)\cos\alpha \tag{17}$$

$$\begin{aligned} I^2_{\text{S1\_RMS}} &= \frac{1}{2\pi}\int_{\omega t_2}^{2\pi+\omega t_1} N_p i_p^2 d\omega t \\ &= \frac{\hat{I}_s^2}{16\pi}\left[\left(\frac{1}{2}-k^2\right)(\pi-2\alpha) - \frac{k}{3}\cos(3\alpha)\right] \end{aligned} \tag{18}$$

Similarly, the instantaneous, average and RMS currents of the device S_2, D_1 and D_2 are obtained correspondingly, where the average and the square of RMS currents of the four power devices are summarized in Table II. Substituting the device instantaneous currents, average currents and RMS currents into (11), (13) and (14), the average power losses of power semiconductor devices can be calculated and compared with the simulation as shown in Fig. 4. When $P > 0$ (inverter mode), the device S_2 is dominated in terms of both conduction and switching losses, as shown in Figs. 4(c) and (g). On the contrary, when $P < 0$ (rectifier mode), the conduction loss is dominated by the device D_2 while S_1 has the maximum switching loss as shown in Figs. 4(d) and (e). The calculated results are coincided with the simulation in Fig. 4.

B. Power Losses of the Capacitor Banks

The MMC station in an HVDC transmission system frequently employs high-power film capacitors as the capacitor bank of the SM. The power losses in capacitors are generally

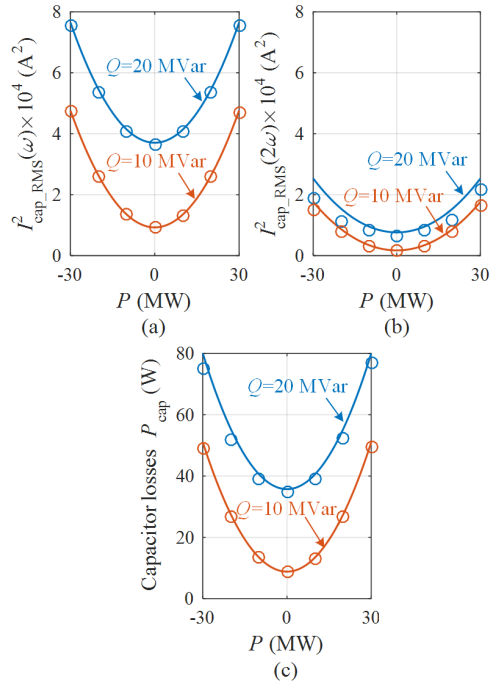


Fig. 5. Comparison of ripples currents and power losses of a capacitor bank under different P/Q set points, where smooth curves are theoretical values and the dots "○" are from simulations: (a) 1st-order ripple currents, (b) 2nd-order ripple currents, and (c) capacitor power losses.

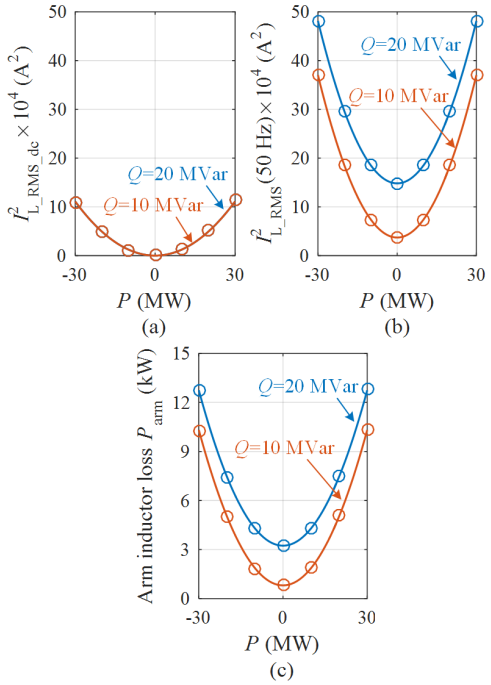


Fig. 6. Comparison of arm inductor currents and power losses under different P/Q set points, where the smooth curves are theoretical values, and the dots "○" are simulated results: (a) DC-component inductor currents, (b) 1st-order inductor currents, and (c) inductor power losses.

composed of Joule losses and dielectric losses, that is

$$\begin{aligned} P_{\text{cap}} &= P_{\text{cap,j}} + P_{\text{cap,d}} \\ &= \sum_{\omega=0}^{\infty} I_{\text{cap\_RMS}}^2(\omega) \cdot R_{\text{s\_cap}} + \sum_{\omega=0}^{\infty} I_{\text{cap\_RMS}}^2(\omega) \cdot \frac{\tan\delta_0}{\omega C} \end{aligned} \tag{19}$$

where $I_{\text{cap\_RMS}}$ is the RMS value of the capacitor current, $R_{\text{s\_cap}}$ is the capacitor series resistance, $\tan\delta_0$ is the dielectric loss factor, C is the capacitance of the selected capacitor and ω is the angular frequency, respectively.

Referring to (7) and (10), the RMS capacitor currents are calculated as

$$\begin{aligned} i_{\text{cap\_p}}(t) &= N_{\text{p}}(t) \times i_{\text{p}}(t) = i_{\text{cap\_p}}(\omega t) + i_{\text{cap\_p}}(2\omega t) \\ &= \underbrace{-\frac{mk\hat{I}_{\text{s}}}{4}\sin(\omega t) + \frac{\hat{I}_{\text{s}}}{4}\sin(\omega t - \varphi_c)}_{\text{fundamental component}} \\ &\quad + \underbrace{\frac{m\hat{I}_{\text{s}}}{8}\cos(2\omega t - \varphi_c)}_{\text{2nd component}} \end{aligned} \tag{20}$$

$$\begin{aligned} i_{\text{cap\_n}}(t) &= N_{\text{n}}(t) \times i_{\text{n}}(t) = i_{\text{cap\_n}}(\omega t) + i_{\text{cap\_n}}(2\omega t) \\ &= \underbrace{\frac{mk\hat{I}_{\text{s}}}{4}\sin(\omega t) - \frac{\hat{I}_{\text{s}}}{4}\sin(\omega t - \varphi_c)}_{\text{fundamental component}} \\ &\quad + \underbrace{\frac{m\hat{I}_{\text{s}}}{8}\cos(2\omega t - \varphi_c)}_{\text{2nd component}} \end{aligned} \tag{21}$$

where $i_{\text{cap\_p/n}}(\omega t)$ and $i_{\text{cap\_p/n}}(2\omega t)$ are the fundamental component and the 2nd-order component in the upper/lower-arm capacitor current.

Consequently, the RMS capacitor currents are calculated as

$$I_{\text{cap\_RMS}}^2(\omega) = \frac{1}{32}\hat{I}_{\text{s}}^2\left(m^2k^2 - 4k^2 + 1\right) \tag{22}$$

$$I_{\text{cap\_RMS}}^2(2\omega) = \frac{1}{128}\hat{I}_{\text{s}}^2 m^2 \tag{23}$$

Substituting (22) and (23) into (19), the corresponding capacitor losses are obtained.

In this case, a high power film capacitor (AVX DK-TFM4#H2657, 3500 V/2.65 mF) is selected as the capacitor bank of the SM. Then, the RMS currents and power losses of the capacitors are shown in Fig. 5, where the smooth curves come from the proposed analytical model and the dots are simulation results. According to Figs. 5(a) and (b), the fundamental-frequency capacitor currents are larger than the currents at the 2nd-order. Under $P = 30$ MW and $Q = 20$ MVar, the RMS value of the fundamental-frequency capacitor current is around four times than the 2nd-order component. Furthermore, the capacitor losses are shown in Fig. 5(c). The capacitor losses increase with both active power and reactive powers. Finally, all the analytical results coincide with the simulated results well.

C. Power Losses of the Arm Inductors

In an MMC-based HVDC transmission, air-core reactors are widely used to avoid saturation. Thus, the power losses of the

TABLE III
SPECIFICATIONS AND PARAMETERS OF A DOWN-SCALE MMC PROTOTYPE

Parameters and Symbols	Values and units
Nominal apparent power S_N	15 kVA
Nominal active power P_N	13.5 kW
DC bus voltage U_{dc}	900 V
Switching frequency f_{sw}	2 kHz
Leakage reactance of the transformer L_T	4 mH (0.12 p.u.)
Arm reactance L_0	4 mH (0.12 p.u.)
SM capacitance C	1640 μF
Grid line voltage at PCC U_s	380 V
Number of SMs per arm N	4
Bleeding resistor of each SM R_b	12 kΩ
IGBT module	1.2 kV/50 A (F4-50R12KS4)
Capacitor C_{SM}	400 V/820 μF (LXS61ZM3M)

TABLE IV
EXPERIMENTAL MEASUREMENTS OF THE SELECTED DEVICES IN THE DOWN-SCALE MMC

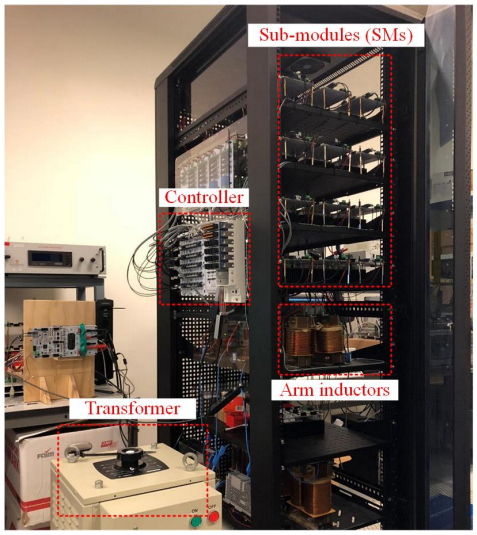
		IGBT	Diode
$U_{cond0@T_{ref}}$	[V]	1.87	1.31
$r_{cond0@T_{ref}}$	[Ω]	3.16E-2	1.46E-2
K_{T1}	[V/°C]	2.70E-3	-3.3E-3
K_{T2}	[Ω/°C]	9.73E-5	1.82E-5
K_i	[1]	1.30	3.32E-1
K_u	[1]	1.33	1.72
K_{sw}	[1/°C]	2.76E-3	1.84E-2
E_{swref}	[mJ]	0.72	0.26
I_{ref}	[A]	20	20
U_{ccref}	[V]	300	300
T_{ref}	[°C]	25	25
		Capacitor	
		@50 Hz	@100 Hz
ESR	[mΩ]	115	89.6
		Inductor	
		@0 Hz	@50 Hz
ESR	[mΩ]	64.4	66.9

arm inductors mainly depend on the winding losses P_w, which is expressed as

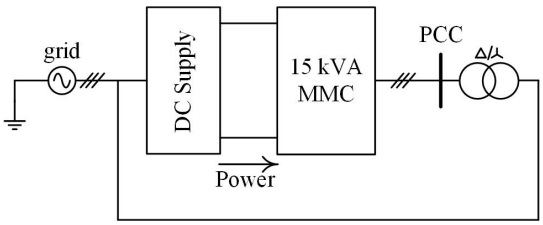
$$P_{arm} = P_w = \sum_{\omega=0}^{\infty} i^2_{arm\_RMS}(\omega) R_{sL}(\omega) \quad (24)$$

where R_{sL} is the equivalent series resistance of the arm inductor and i_{arm_RMS} is the RMS current.

According to (7), the arm currents through the arm inductors consist of a dc component and a fundamental-frequency current. Under different P/Q set points, the two components of the arm current are shown in Figs. 6(a) and (b). The dc components increase with active power while it is independent of the reactive power. For the 50 Hz component, the RMS values of the arm currents accelerate with the rising of active power and reactive power. However, it should be noted that the 50-Hz component is around 5 times than the dc component, which indicates that the 50-Hz arm current generates the most part of power losses in the arm inductor. Then, the arm inductor losses are shown in Fig. 6(c). The simulation results coincide with the theoretical results.



(a)



(b)

Fig. 7. The experimental platform of the the downscale MMC: (a) the platform photo and (b) the circuit configuration.

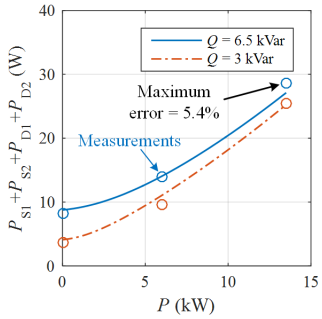


Fig. 8. The total power losses of the four power semiconductor devices in an SM of the downscale platform (smooth curves: the results based on the proposed analytical model; the dots "○": experimental results).

IV. EXPERIMENTAL VERIFICATIONS

In order to verify the effectiveness of the proposed analytical model, an experimental platform has been built as shown in Fig. 7. The 15 kVA down-scale MMC is connected to the grid via an isolated transformer. Three 4 mH (0.12 p.u.) AC inductors are utilized as the leakage inductance of the transformer. The grid voltage at the secondary transformer is selected as PCC. The detailed parameters are listed in Table III. In the down-scale MMC prototype, each phase has two arms and each arm consists of 4 SMs. In each half-bridge SM, a 1200 V/50 A IGBT module is used. Two electrolytic

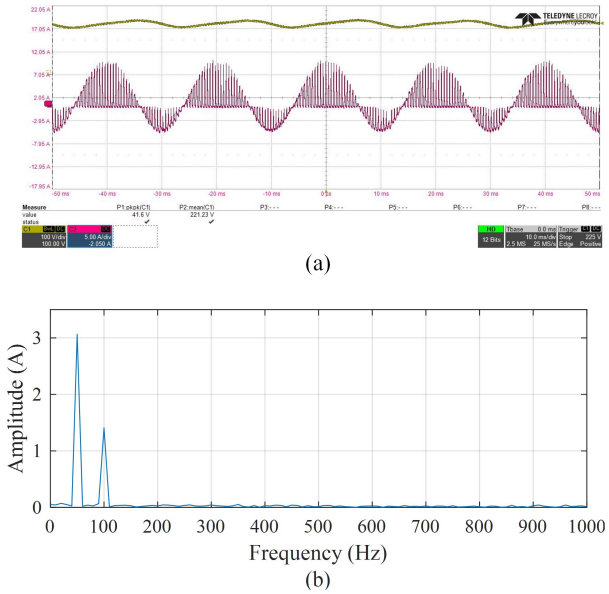


Fig. 9. Waveforms of the SM capacitor: (a) the capacitor voltage and current and (b) FFT analysis of the capacitor current.

capacitors (820 μF $\times$ 2) are chosen in the SM due to the constraint of the converter volume, although the film capacitor is utilized more widely for HVDC applications.

A. The Power Losses of the IGBT Module

In the first step, the power loss-related coefficients as presented in (11) and (12) are obtained experimentally listed in Table IV. Since it is difficult to measure the power losses of a single power semiconductor chip, the whole IGBT-module power losses are measured by the Newtons Power Analyzer PPA5500. The calculated and measured power losses are shown in Fig. 8. When the active power is increasingly injected to the grid, the power losses of the IGBT module are rising. At the same time, the reactive power (from 3 kVar to 6.5 kVar) also boosts the power losses of the IGBT module. The measurements coincide with the results based on the proposed analytical model. The maximum error is 5.3%.

B. Capacitor Power Losses

As listed in Table IV, the measured capacitor equivalent series resistances are 115 mΩ (50 Hz) and 89.6 mΩ (100 Hz), respectively. These resistances decrease with the frequency. Then, the voltage and current of an SM capacitor are measured as shown in Fig. 9. Based on the FFT analysis of the capacitor current as shown in Fig. 9(b), the major capacitor currents are fundamental and second-order components, which verifies (19). Then, the capacitor currents and power losses are summarized in Fig. 10 with different active/reactive power. The measured capacitor currents are closely matched with the analytical models as shown in Figs. 10(a) and (b). The experimental power loss data also agrees with the theoretical values in a small error, with a maximum error of 8.2%. This kind of error might come from the switching-frequency ripple currents, which are neglected in the analytical model.

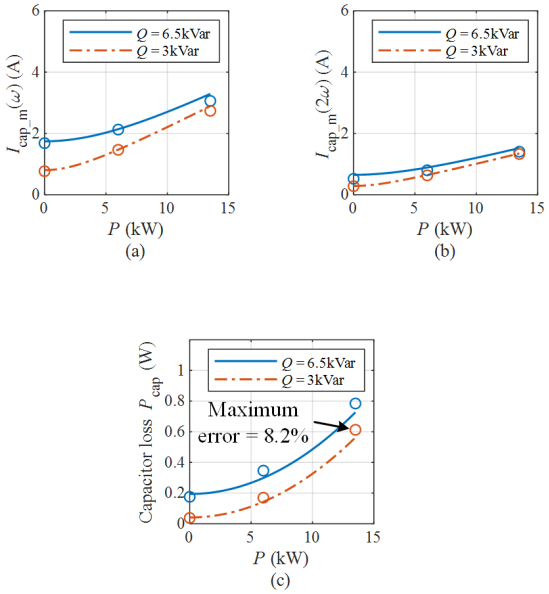


Fig. 10. The experimental capacitor losses (smooth curves: the results based on the proposed analytical model; the dots "○": experimental results): (a) 1st-order ripple currents, (b) 2nd-order ripple currents, and (c) capacitor power losses.

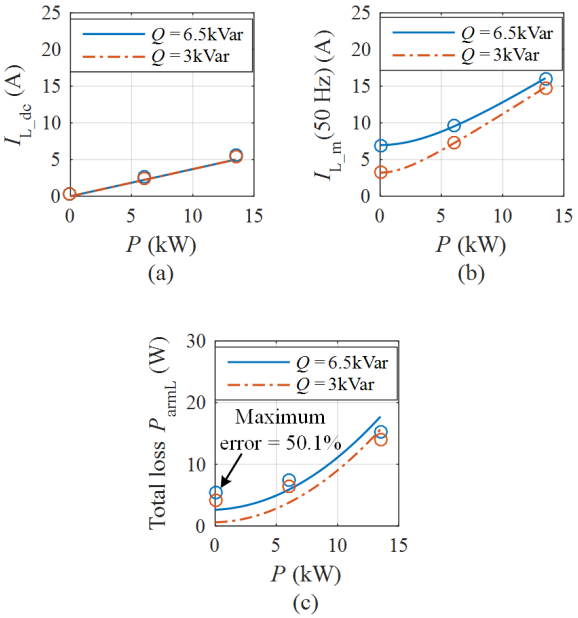


Fig. 11. The experimental capacitor losses (smooth curves: the results based on the proposed analytical model; the dots "○": experimental results): (a) DC-component inductor currents, (b) 1st-order inductor currents, and (c) inductor power losses.

C. Inductor Power Losses

Due to the consideration of power density, the down-scale MMC platform uses the iron-core arm inductors rather than

the air-core type. Therefore, apart from the winding loss in (24), the core loss is also an important part and expressed as

$$P_{\text{core}} = \left(C_{\text{dc}} K_{\text{h}} f \hat{B}^2 + K_{\text{c}} f^2 \hat{B}^2 + K_{\text{e}} f^{1.5} \hat{B}^{1.5} \right) \cdot V_{\text{c}} \quad (25)$$

$$C_{\text{dc}} = \sqrt{K_{\text{dc}} \left| B_{\text{dc}} \right| \Big/ \hat{B} + 1} \quad (26)$$

where $\hat{B}$ is the amplitude of the ac flux component with the frequency f, K_{h} is the hysteresis core loss coefficient, K_{c} is the eddy-current core loss coefficient, K_{e} is the excess core loss coefficient, and V_{c} is the volume of the core. Note that an inherent dc-bias current exists in the arm current of the MMC, the coefficient C_{dc} helps to consider the impact of the biased magnetization. The measured inductor currents and power losses are shown in Fig. 11. The arm inductor current is dominated by a dc component and an ac component at the fundamental frequency. As shown in Fig. 11(a), the dc component is independent of reactive power and linearly increases with the active power. On the contrary, the AC current at 50 Hz is affected by both active and reactive powers as shown in Fig. 11(b). Both measured currents are closely matched with the corresponding analytical results. Moreover, the power losses of an arm inductor are illustrated in Fig. 11(c). The measured inductor power losses are very close to their theoretical estimation, but the estimation is relatively small when P=0 kW while the estimation is larger when P=13.5 kW. The errors are probably from the core loss model without considering the harmonics. Although the estimated error is up to 50.1% when the active power is zero, the estimated power losses are acceptable since the power loss value is relatively small under the conditions. A more comprehensive power loss model of the arm inductor is necessary, which should further consider the impact of the switching-frequency components.

V. Conclusion

For better component sizing and reliability assessment, a systematic power loss evaluation is a fundamental requirement for the MMC. This paper has established analytical power-loss models of the power semiconductor devices, capacitors, and inductors. All the electrical parameters are based on the P/Q set points with PCC of the grid. Moreover, the reactive power consumption of the leakage inductance of the AC transformer is also considered. The established model is computation-efficient and parameter-changing friendly. Then, both a 36-MVA MMC simulation model and a 15-kVA experimental platform are employed for validation. The simulation and measured results verify the effectiveness of the proposed model. Comparison of the measurements and the theoretical values, the maximum errors of power devices and capacitors are 5.4% and 8.2%, respectively. The maximum error of inductor power losses is relatively large as 50.1% when the active power is zero. However, the estimated power losses of the arm inductors are still acceptable because the power loss values are small in the condition, which imposes a further study to consider the impacts of switching-frequency components on the arm inductors of MMCs.

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